ABSTRACT OF THE INVENTION

The present invention is a class of circuits named asynchronous pulse logic (APL) circuit and designing methods for such circuits. APL replaces two of the four-phase handshakes in QDI circuits with pulses, thus breaking the timing dependencies that cause performance problems in QDI circuits. Since the pulse length in APL varies so little, it can be assumed constant. This assumption frees designers from needing to consider the effects of the inputs and outputs on the pulse length, which means timing properties can be verified locally. One embodiment of the present invention is a class of circuit design called the single-track-handshake-asynchronous-pulse-logic (STAPL), which serves as a new target for the compilation of CHP (Communication Hardware Process) programs. In one embodiment, a five-stage pulse generator is used to create a 10 transition count cycle circuit. Advantages of STAPL include a simplified solution to the charge-sharing problem and less loading from p-transistors.